

# **Agilent W2637A, W2638A, and W2639A**

**LPDDR BGA Probes and  
Oscilloscope Adapter Board**

**User's Guide**



**Agilent Technologies**

## Notices

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# Contents

## **Contents 3**

### **Introduction 4**

W2637A and W2638A LPDDR BGA Probes Description 4

Technical Feature Summary 5

Why Use LPDDR? 5

Top Views 6

Equipment Supplied / Required 7

Mechanical Considerations 9

Dimensions 12

### **Installing the LPDDR BGA Probes 14**

Soldering the Probe 14

Logic Analyzer Connection to the LPDDR probes 15

W2637A Probe Pin-Out 18

W2638A Probe Pin-Out 19

Probing with the W2639A and an InfiniiMax Probe 23

Oscilloscope Connection to the LPDDR Probes 23

W2639A Oscilloscope Adapter Board Pin-Outs 26

### **Setting Up the Logic Analysis System 31**

To Save a Configuration File 31

### **Characteristics, Regulatory, and Safety Information 32**

SPIICE Decks 34

Operating Characteristics 38

Safety Notices 39

Regulatory Notices 40

### **Appendix: W2639A Rework Instruction Guide 41**

## 1. Introduction

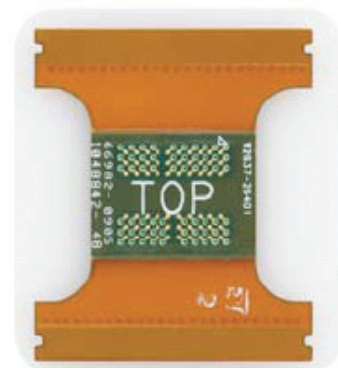
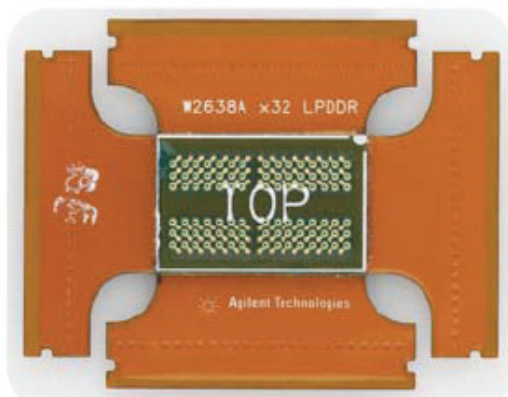
This document provides information for the following Agilent products:

- W2637A LPDDR Probe (x16)
- W2638A LPDDR Probe (x32)
- W2639A Oscilloscope Adapter Board

The LPDDR (Low Power DDR) DRAM BGA probes enable logic analyzer state and timing measurements of all the DRAM buses, including the DQ, DQS, and clock signals of x16 and x32 DRAMs using the JEDEC standard common LPDDR DRAM footprint.

The probes interpose between the DRAM being probed and the PC board where the DRAM would normally be soldered. The probe is designed to be soldered to the PCB footprint for the DRAM. The DRAM being probed is then soldered to the top side of the probe.

Each DRAM signal in the common footprint (including those defined for x16 and x32 DRAMs) passes directly from the bottom side of the probe to the top side of the probe. Buried probe resistors placed at the DRAM balls connect the probed signals to the rigid flex to mate with an Agilent cable adapter (ZIF probe). The W2637A/38A probes are also compatible with the Agilent InfiniiMax oscilloscope probes (E2678A single-ended/differential socketed probe heads). This allows oscilloscope probing of the DRAM signals with an Infiniium 80000 or 90000A Series oscilloscope, giving you a LPDDR testing solution covering the clock characterization, electrical and timing parameters of the JEDEC specification.



## Technical Feature Summary

- Probing of LPDDR x16 and x32 DRAMs in BGA package using JEDEC standard common BGA footprint.
- Logic analyzer (using E5384A/E5826 single-ended ZIF probe) and oscilloscope (using E2678A InfiniiMax socketed probe head) connection to RAS#, CAS#, WE#, DQ, DQS/DQS#, and CK/CK# signals.
- Differential or single ended probing of DQS and CLK signals.
- Interposer design probes signals between DRAM BGA balls and DIMM.
- Use of separate E5384A and E5826A single ended probes for connection to the logic analyzer optimizes use of analyzer channels by allowing assignment of analyzer channels to 8 or 16 bits on each DRAM.
- Tin plating of the DRAM footprint on the top side of the probes is compatible with leaded and no-lead DRAM balls.
- Easy oscilloscope probing (no soldering) through ZIF connections and socketed probe heads.

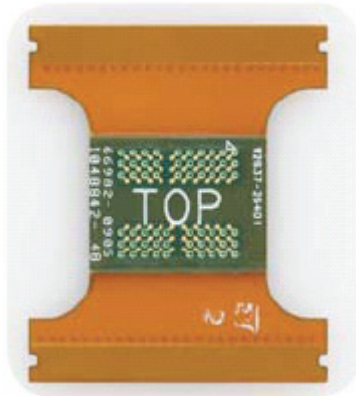
## Why is LPDDR Used?

- Many embedded designs do not require the performance of DDR2 or DDR3.
- Do not want to change or re-design memory interface architecture.
- Requires little investment to bring down device power consumption.
- New applications – cell phones, networking devices, portable devices, etc.

## 1. Introduction

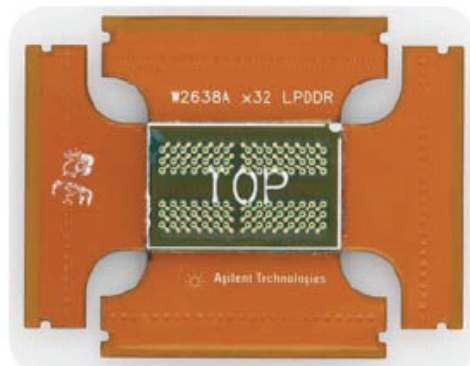
The following pictures show the W2637A and W2638A BGA probes, and the W2639A Oscilloscope Adapter Board.

### W2637A Top View



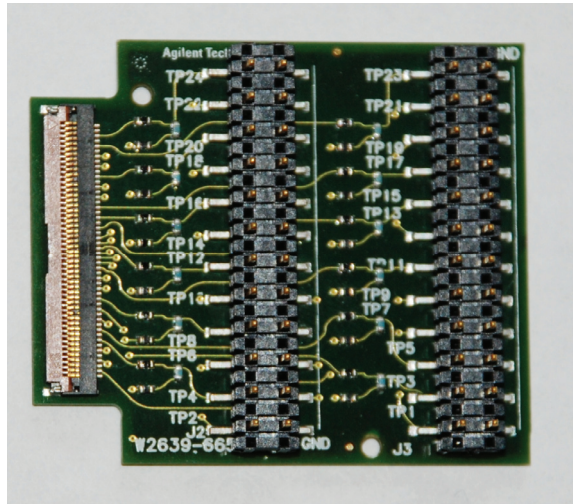
Top view (DRAM  
attach side)

### W2638A Top View



Top view (DRAM  
attach side)

## W2639A Top View



Top view

## Equipment Supplied

### W2637A and W2638A LPDDR BGA Probes

The following components have been shipped with your W2637A or W2638A LPDDR BGA probe (the first bullet shows the various ordering options and the number / type of probe(s) included with each):

- W2637A-101: kit of one W2637A LPDDR probe  
W2637A-102: kit of two W2637A LPDDR probes  
W2637A-104: kit of four W2637A LPDDR probes  
W2638A-101: kit of one W2638A LPDDR probe  
W2638A-102: kit of two W2638A LPDDR probes  
W2638A-104: kit of four W2638A LPDDR probes
- This *User's Guide*.

### W2639A Oscilloscope Adapter Board

- Each W2639A Oscilloscope Adapter Board order includes two oscilloscope adapter boards. Therefore, since the W2637A probe only uses two boards you will need to order W2639A once and since the W2638A probe uses four boards, you will need place two orders for W2639A.

### Equipment Required (when using probes with logic analyzer)

This section provides the configuration guide for probing x16 and x32 DRAM type with various data width. You will need:

- Agilent 16900-series logic analyzer system
- An appropriate number of Agilent logic analyzer cards connected together as a module.

#### Logic Analyzer Configuration Guide

DRAM type	Data width	Access to signals	Access to signals	Cables	Logic Analyzer	Order summary
X16	X16	Command, Address, and Data	W2637A	E5384A	16950Bx1	16950B: 1 E5384A: 1 W2637A
X32	X32	Command, Address, and Data	W2638A	E5384A	16950Bx2	16950B: 1 E5384A: 1 E5826A: 1 W2638A
		Data		E5826A		

### Equipment Required (when using probes with oscilloscope)

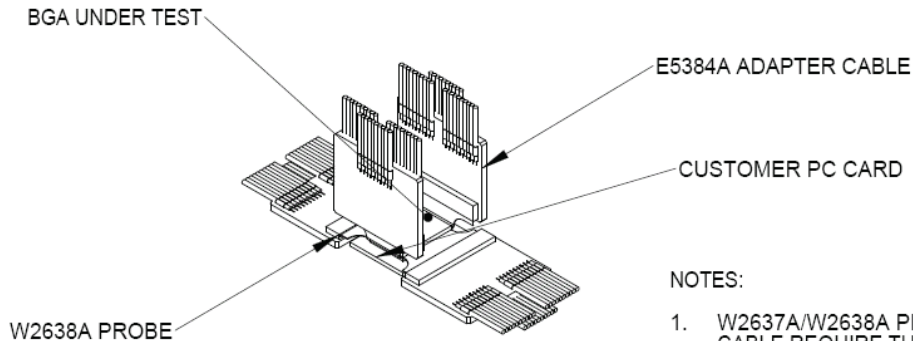
In order to use the LPDDR BGA probes with an Infiniium oscilloscope, you will need the following equipment:

- If using W2637A: W2639A (x1)  
If using W2638A: W2639A (x2)
- Agilent 80000 or 90000A Series oscilloscope
- Agilent InfiniiMax probe amplifier with E2678A single ended / differential socketed probe head and accessories



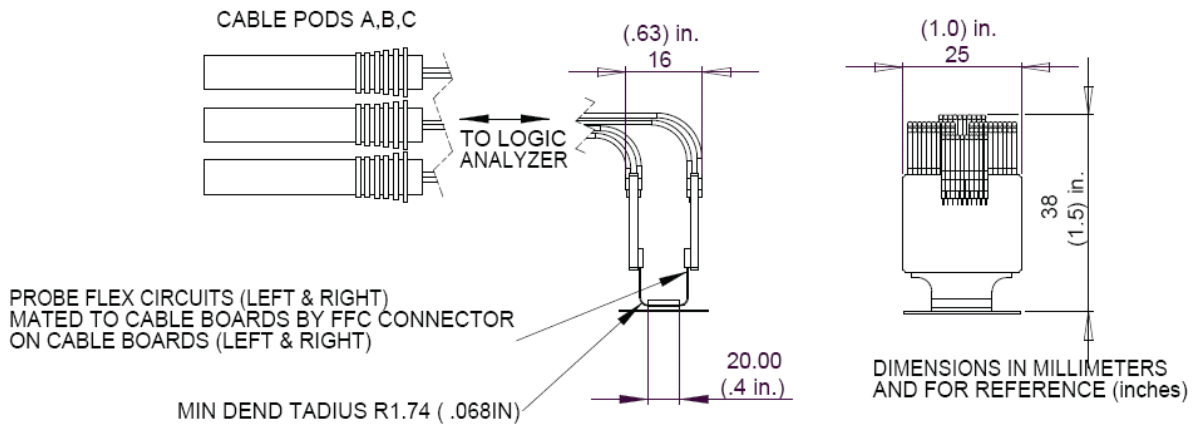
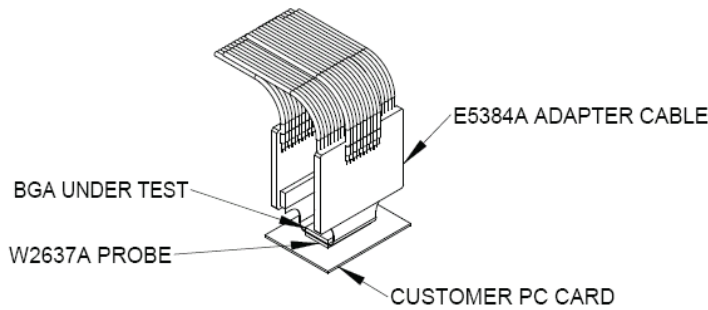
## Mechanical Considerations

The following figures show the Keep Out Volume for various logic analyzer cables / adapters / probes when connected to the LPDDR Probes or the Oscilloscope Adapter Board.

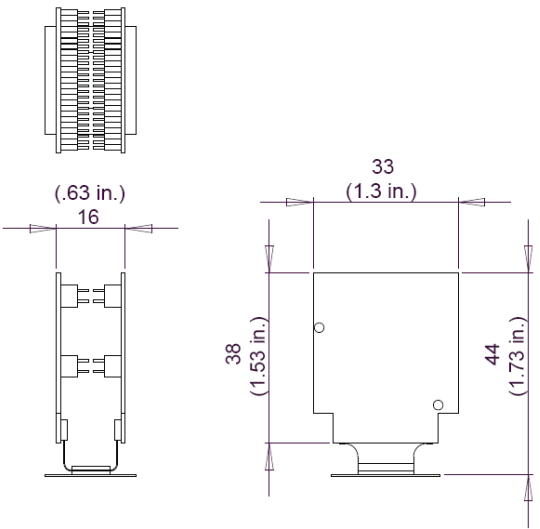
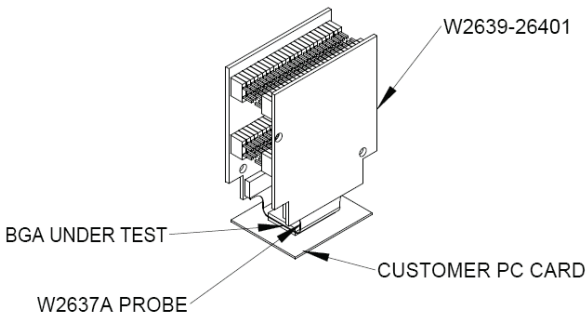
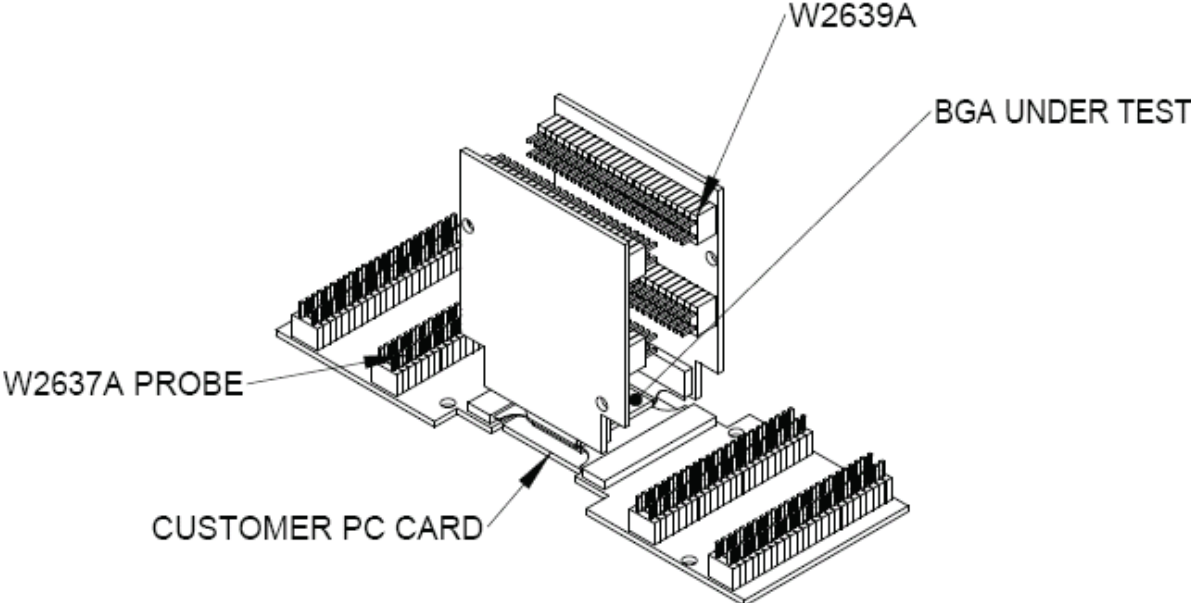


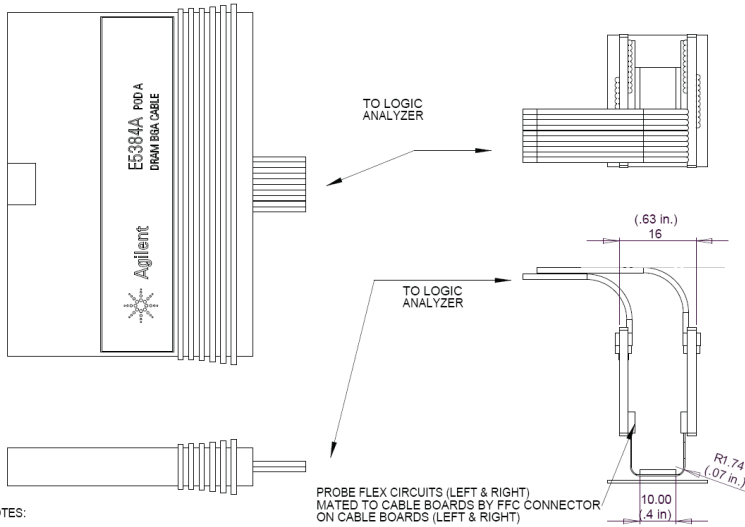
NOTES:

1. W2637A/W2638A PROBE AND E5384 ADAPTER CABLE REQUIRE THE X,Y,Z SPACE DEPICTED ON THIS DRAWING
2. KEEPOUT VOLUME WIDTH (16) IS SPECIFIED PER MINIMUM BEND RADIUS OF PROBE FLEX, WIDTH WILL BE 54 mm (2.10 in.).



1. Introduction

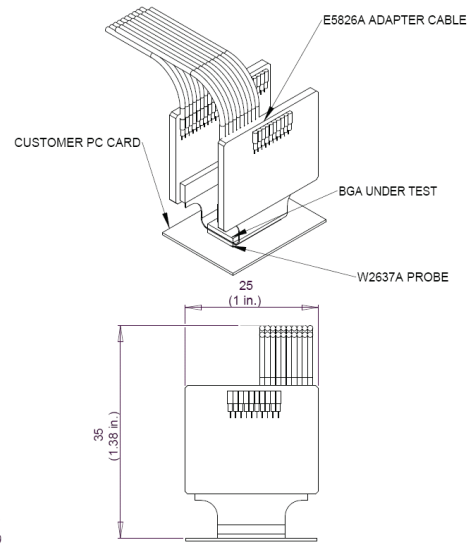




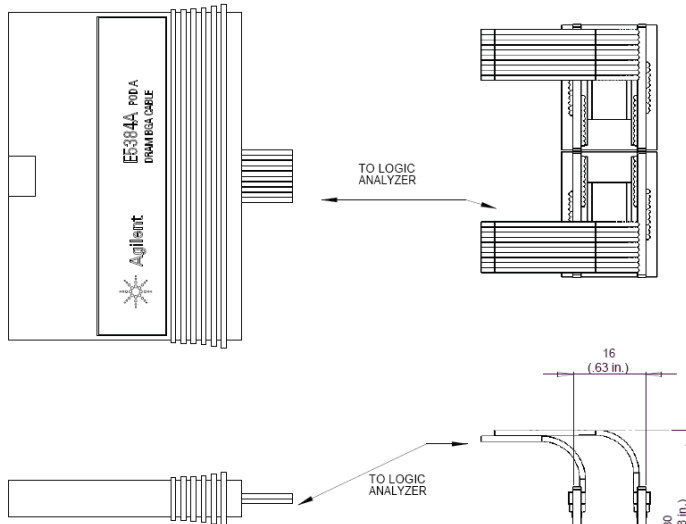
NOTES:

1. W2637A/W2638A PROBE WITH ADAPTER CABLE E5384A REQUIRE THE X,Y,Z SPACE DEPICTED ON THIS DRAWING
2. KEEP-OUT VOLUME WIDTH (16) IS SPECIFIED PER MINIMUM BEND RADIUS OF PROBE FLEX 1.74mm. WIDTH WILL BE 54 mm (2.10 in.).

PROBE FLEX CIRCUITS (LEFT & RIGHT) MATED TO CABLE BOARDS BY FFC CONNECTOR ON CABLE BOARDS (LEFT & RIGHT)



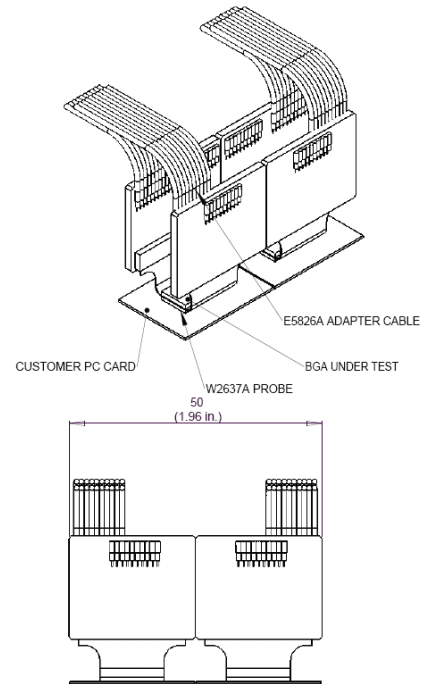
DIMENSIONS IN MILLIMETERS AND FOR REFERENCE (inches)



NOTES:

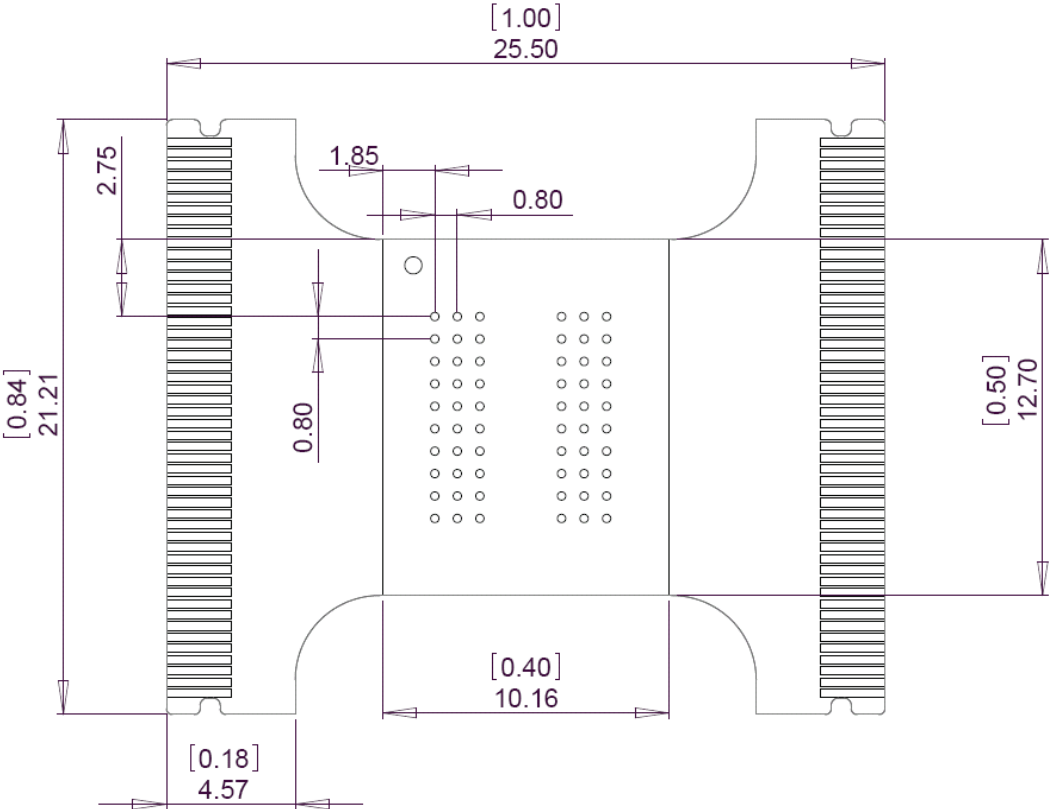
1. W2637A/W2638A PROBE WITH ADAPTER CABLE E5384A REQUIRE THE X,Y,Z SPACE DEPICTED ON THIS DRAWING
2. KEEP-OUT VOLUME WIDTH (16) IS SPECIFIED PER MINIMUM BEND RADIUS OF PROBE FLEX 1.74mm. WIDTH WILL BE 54 mm (2.10 in.).

PROBE FLEX CIRCUITS (LEFT & RIGHT) MATED TO CABLE BOARDS BY FFC CONNECTOR ON CABLE BOARDS (LEFT & RIGHT)

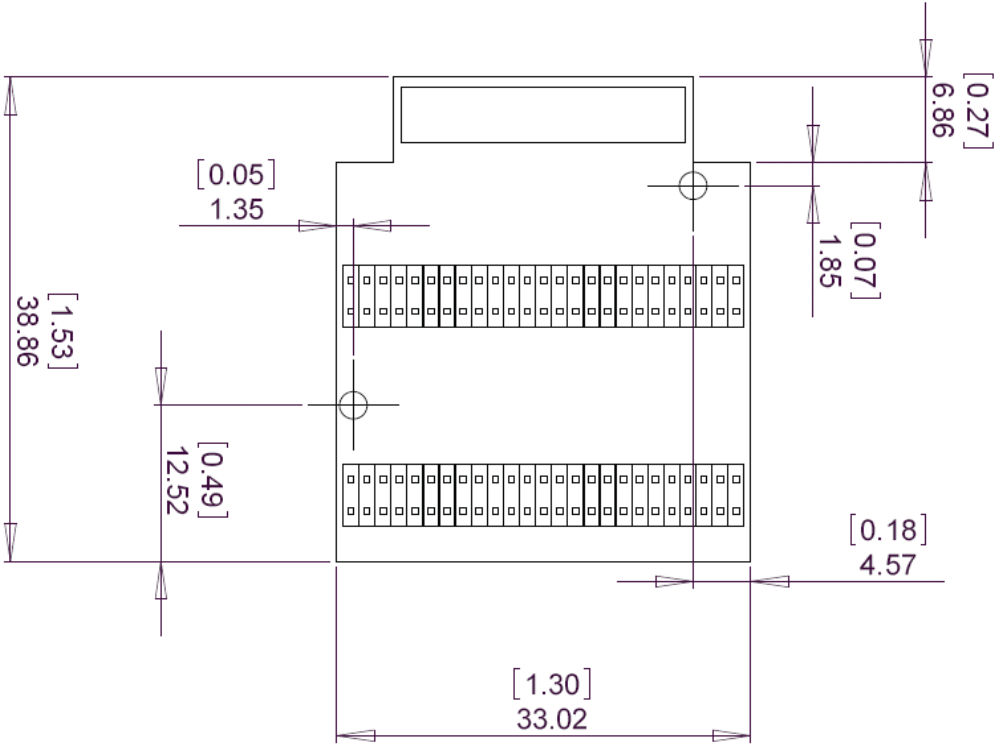


DIMENSIONS IN MILLIMETERS AND FOR REFERENCE (inches)

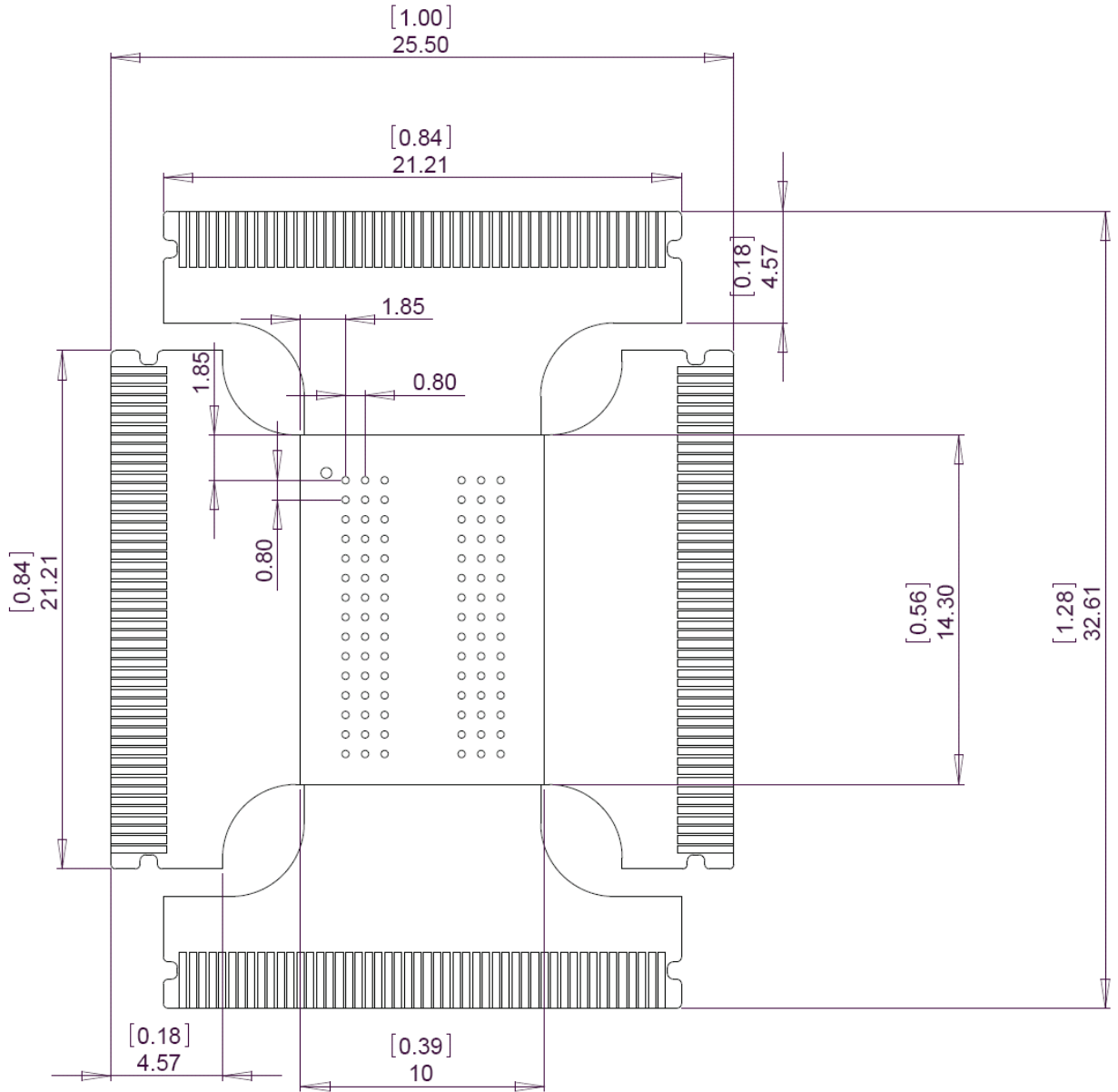
1. Introduction



W2637A



W2639A



**W2638A**

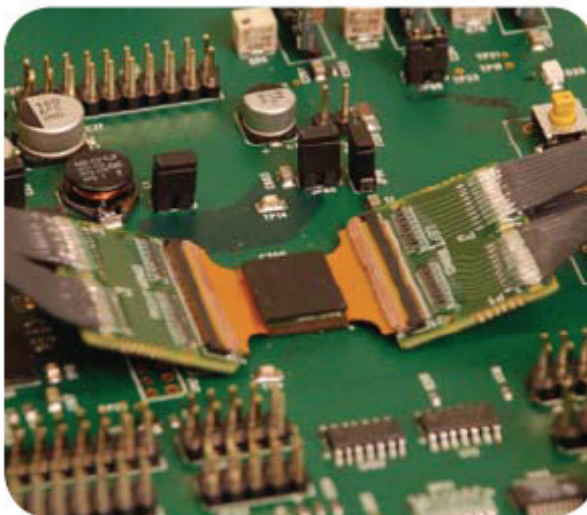
## 2. Installing the LPDDR BGA Probes

### Soldering the probe

The W2637A/38A BGA probes need to be attached to the DRAM PCB footprint on the design to be probed, and the desired DRAM is soldered to the top side of the probe. This attachment may occur in any order (i.e. first solder the probe to the DUT and then solder the DRAM to the probe, or first solder the DRAM to the probe and then solder the DRAM+probe assembly to the DUT). The probes are designed to tolerate lead-free soldering temperature profiles. However, it is always recommended to apply the minimum temperature required and the minimum number of heating/cooling cycles to reduce risk of any damage to the probes.

The probes are supplied without solder balls. Depending on the exact attachment order, either leaded or lead-free solder may be preferred to attach the probe to the DUT. The design of the probe supports either choice.

The flexible “wings” on the probes may need to be bent upwards before soldering to avoid mechanical contact with components adjacent to the probe on the DUT. This will ensure reliable connection when connected to the logic analyzer cable adapters.

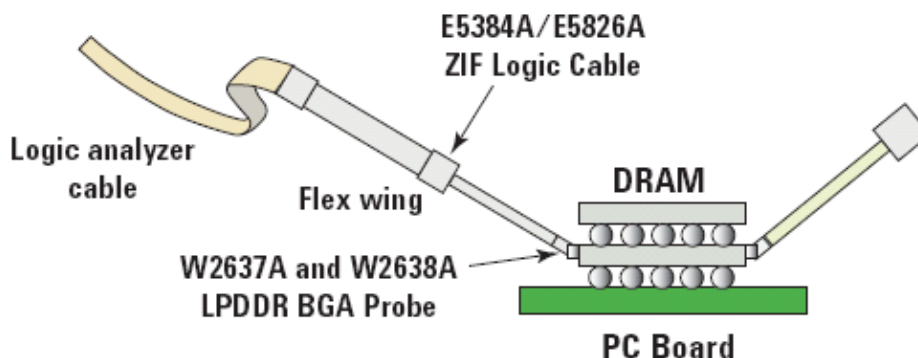


If you do not have the in-house expertise to attach the BGA probe adapter and DRAM, contract manufacturers with this expertise may be willing to perform the attachment for a fee. More information on BGA soldering and rework techniques that may be useful in attaching the probe can be found at:

- <http://www.circuitrework.com/guides/9-0.shtml>
- <http://www.agilent.com/find/lpddrbga>

## Logic Analyzer Connection to the LPDDR Probes

The W2637A LPDDR BGA probe connects to E5384A to provide connection to the logic analyzer for the x16 LPDDR package. The W2638A LPDDR BGA probe connects to E5384A and E5826A to provide connection to the logic analyzer for the x32 LPDDR package. The E5384A and/or E5826 plug into the 90-pin logic analyzer pod cable.



**LPDDR x16 E5384A Probe Cable Pin Assignment**

Data Pod		
Logic Channel	Signal Name	BGA Ref
0	DQ6	D8
1	DQ9	D2
2	DQ4	C8
3	DQ8	E3
4	DQ11	C2
5	DQ7	E7
6	DQ10	D3
7	DQ5	D7
8	DQ1	B7
9	DQ15	A2
10	DQ2	B8
11	DQ13	B2
12	DQ12	C3
13	DQ3	C7

Control Pod		
Logic Channel	Signal Name	BGA Ref
0	BA1	H9
1	CAS#	G8
2	WE#	G7
3	RAS#	G9
4	CS#	H7
5	BA0	H8
6	LDQS	E8
7	NC	
8	LDM	F8
9	UDM	F2
10	UDQS	E2
11	NC	
12	-	
13	-	

Address Pod		
Logic Channel	Signal Name	BGA Ref
0	NC	
1	A2	K7
2	A10	J7
3	NC	
4	A3	K8
5	A7	J2
6	A5	K3
7	A0	J8
8	A4	K2
9	A1	J9
10	A6	J1
11	A11	H2
12	A8	J3
13	A12, NC	H3

## 2. Installing the LPDDR BGA Probes

14	DQ14	B3
15	DQ0	A8
Clock_P	CKE	G1
Clock_N	GND	

14	-	
15	-	
Clock_P	CK	G2
Clock_N	CK#	G3

14	A9	H1
15	A13	F7
Clock_P	-	
Clock_N	-	

### LPDDR x32 E5384A and E5826A Probe Cable Pin Assignment

Logic Analyzer Cable #1 (E5384A)

Data Pod		
LA Channel	Signal Name	BGA Ref
0	DQ4	N8
1	DQ11	N2
2	DQ2	P8
3	DQ13	P2
4	DQ15	R2
5	DQ0	R8
6	DQ9	M2
7	DQ6	M8
8	DQ18	B8
9	DQ29	B2
10	DQ20	C8
11	DQ27	C2
12	DQ25	D2
13	DQ22	D8
14	DQ31	A2
15	DQ16	A8
Clock_P	CKE	G1
Clock_N	GND	

Control Pod		
LA Channel	Signal Name	BGA Ref
0	DQS0	L8
1	DM0	K8
2	BA0	H8
3	BA1	H9
4	DQS1	L2
5	DM1	K2
6	RAS#	G9
7	CAS#	G8
8	WE#	G7
9	DM2	F8
10	DQS2	E8
11	DM3	F2
12	-	
13	-	
14	-	
15	-	
Clock_P	CS#	
Clock_N	GND	

Address Pod		
LA Channel	Signal Name	BGA Ref
0	A5	K3
1	A2	K7
2	A10	J7
3	A4	K1
4	A3	K9
5	A11	H2
6	A8	J3
7	A0	J8
8	A7	J2
9	A1	J9
10	A12	H3
11	NC	
12	A6	J1
13	NC	
14	A9	H1
15	NC	
Clock_P	-	
Clock_N	-	



Logic Analyzer Cable #2 (E5826A)

<b>Data Pod</b>		
LA Channel	Signal Name	BGA Ref
0	DQ19	C7
1	DQ3	N7
2	DQ21	D7
3	DQ5	M7
4	DQ7	L7
5	DQ23	E7
6	DQ1	P7
7	DQ17	B7
8	DQ26	D3
9	DQ10	M3
10	DQ28	C3
11	DQ12	N3
12	DQ14	P3
13	DQ30	B3
14	DQ8	L3
15	DQ24	E3
Clock P	CK	G2
Clock N	CK#	G3

## 2. Installing the LPDDR BGA Probes

### W2637A x16 LPDDR BGA Probe Pin-Out

Left Flex Wing (E5384A)			Right Flew Wing (E5384A)		
Pin	Signal Name	Group	Pin	Signal Name	Group
All odd pins	GND	-	All odd pins	GND	-
2	NC	-	100	GND	-
4	DQ14	Data	98	DQ0	Data
6	DQ15	Data	96	DQ1	Data
8	DQ13	Data	94	DQ2	Data
10	DQ12	Data	92	DQ3	Data
12	UDQS	Data	90	GND	-
14	DQ10	Data	88	CKE	Command
16	DQ9	Data	86	DQ5	Data
18	DQ8	Data	84	DQ6	Data
20	DQ11	Data	82	DQ4	Data
22	UDM	Data	80	DQ7	Data
24	LDM	Data	78	CK	Command
26	NC	-	76	CK#	Command
28	LDQS	Data	74	RASH#	Command
30	BAD	Command	72	WE#	Command
32	CS#	Command	70	CAS#	Command
34	A9	Address	68	BA1	Command
36	A7	Address	66	A13	Address
38	A6	Address	64	A12	Address
40	A8	Address	62	A11	Address
42	A4	Address	60	A1	Address
44	A5	Address	58	A0	Address
46	NC	-	56	A10	Address
48	NC	-	54	A3	Address
50	GND	-	52	A2	Address

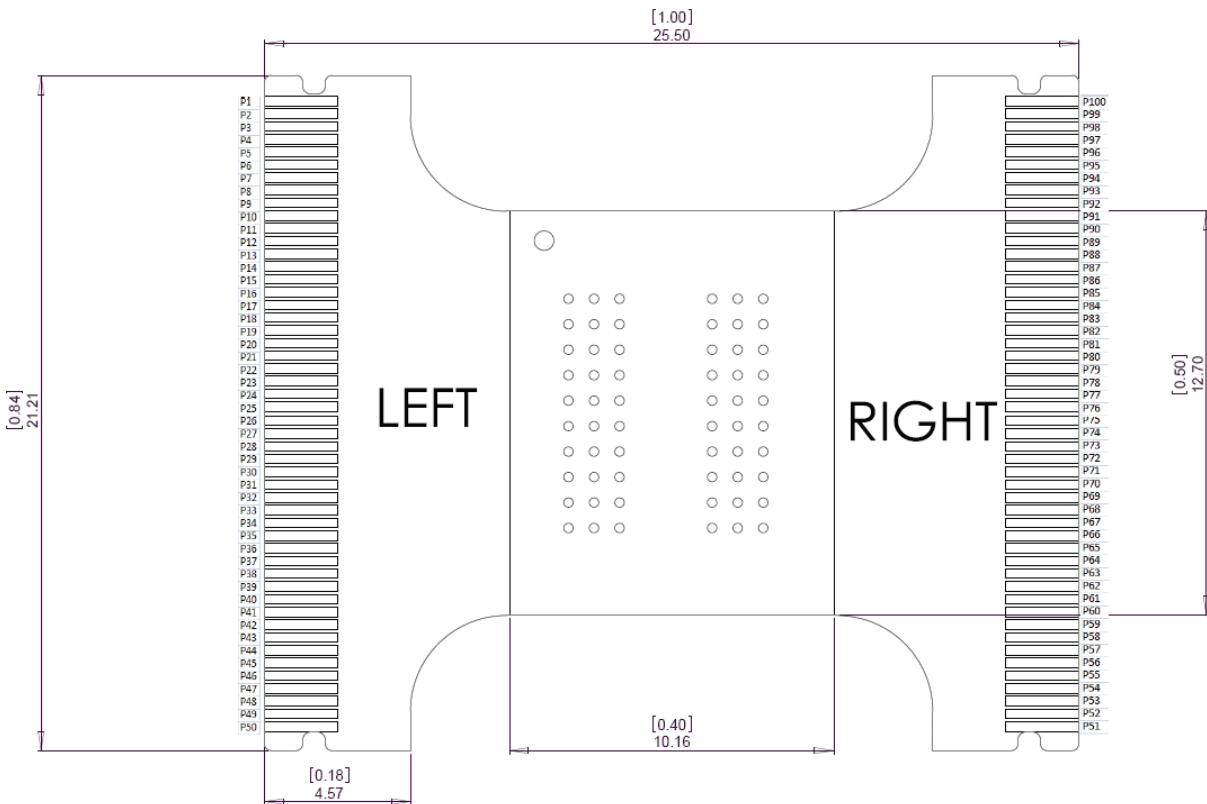
**W2638A x32 LPDDR BGA Probe Pin-Out**

<b>Left Flex Wing (E5384A)</b>			<b>Right Flew Wing (E5384A)</b>		
<b>Pin</b>	<b>Signal Name</b>	<b>Group</b>	<b>Pin</b>	<b>Signal Name</b>	<b>Group</b>
All odd pins	GND	-	All odd pins	GND	-
2	DM3	Data	100	GND	-
4	DQ31	Data	98	DQ16	Data
6	DQ29	Data	96	DQ18	Data
8	DQ27	Data	94	DQ20	Data
10	DQ25	Data	92	DQ22	Data
12	DQS2	Data	90	GND	-
14	DQ9	Data	88	CKE	Command
16	DQ11	Data	86	DQ6	Data
18	DQ13	Data	84	DQ4	Data
20	DQ15	Data	82	DQ2	Data
22	DM2	Data	80	DQ0	Data
24	WE#	Command	78	CS#	Command
26	CAS#	Command	76	GND	-
28	RAS#	Command	74	BA1	Command
30	DM1	Data	72	BA0	Command
32	DQS1	Data	70	DM0	Data
34	A9	Address	68	DQS0	Data
36	A11	Address	66	NC	-
38	A12	Address	64	NC	-
40	A6	Address	62	NC	-
42	A7	Address	60	A1	Address
44	A8	Address	58	A0	Address
46	A4	Address	56	A10	Address
48	A5	Address	54	A3	Address
50	GND	-	52	A2	Address

## 2. Installing the LPDDR BGA Probes

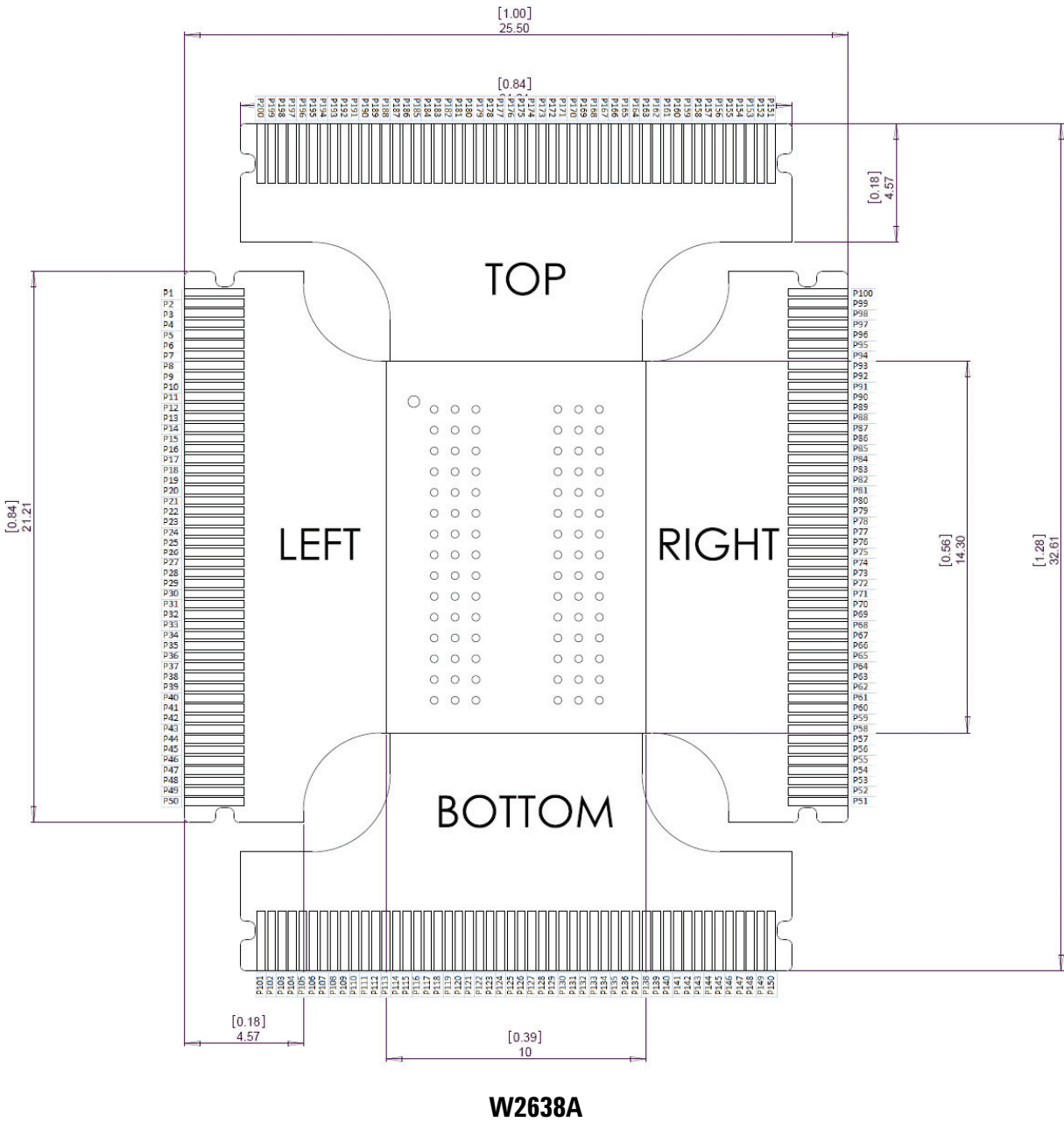
### W2638A x32 LPDDR BGA Probe Pin-Out (continued)

Bottom Flex Wing (E5826A)			Top Flew Wing (E5826A)		
Pin	Signal Name	Group	Pin	Signal Name	Group
All odd pins	GND	-	All odd pins	GND	-
102	NC	-	200	GND	-
104	DQ8	Data	198	DQ24	Data
106	DQ10	Data	196	DQ26	Data
108	DQ12	Data	194	DQ28	Data
100	DQ14	Data	192	DQ30	Data
112	NC	-	190	GK#	Command
114	DQ1	Data	188	CK	Command
116	DQ3	Data	186	DQ17	Data
118	DQ5	Data	184	DQ19	Data
120	DQ7	Data	182	DQ21	Data
122	NC	-	180	DQ23	Data
124	NC	-	178	NC	-
126	NC	-	176	NC	-
128	NC	-	174	NC	-
130	NC	-	172	NC	-
132	NC	-	170	NC	-
134	NC	-	168	NC	-
136	NC	-	166	NC	-
138	NC	-	164	NC	-
140	NC	-	162	NC	-
142	NC	-	160	NC	-
144	NC	-	158	NC	-
146	NC	-	156	NC	-
148	NC	-	154	NC	-
150	GND	-	152	NC	-



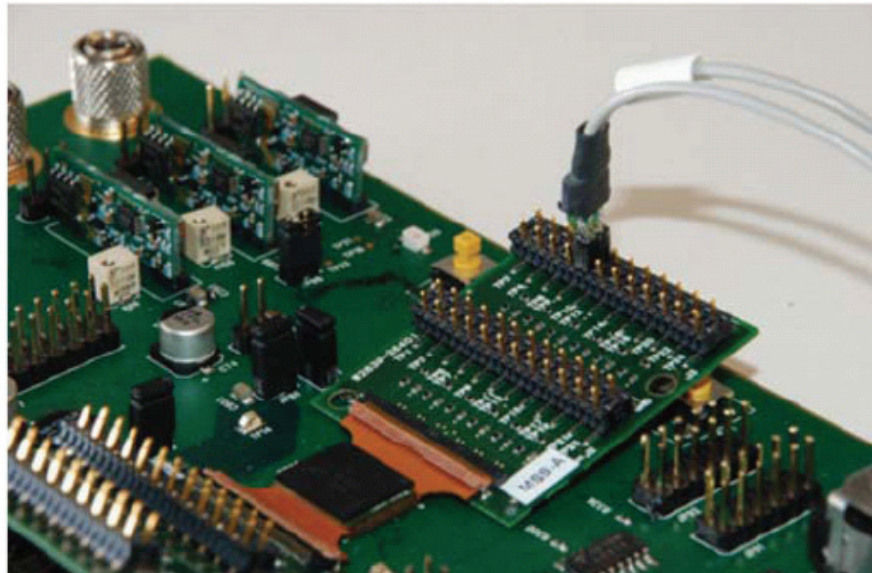
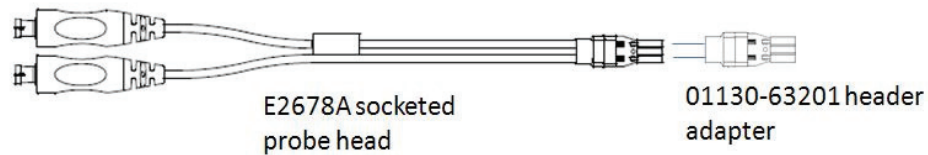
**W2637A**

## 2. Installing the LPDDR BGA Probes



## Probing the W2639A Oscilloscope Adapter Board with an InfiniiMax Probe

The picture below shows the W2637A LPDDR BGA probe connected to an oscilloscope via the W2639A LPDDR oscilloscope probe adapter board and E2678A socketed probe head. Note: The E2678A socketed probe head needs to be used with the damping adapter (01130-63201) to connect to the W2639A oscilloscope probe adapter board.

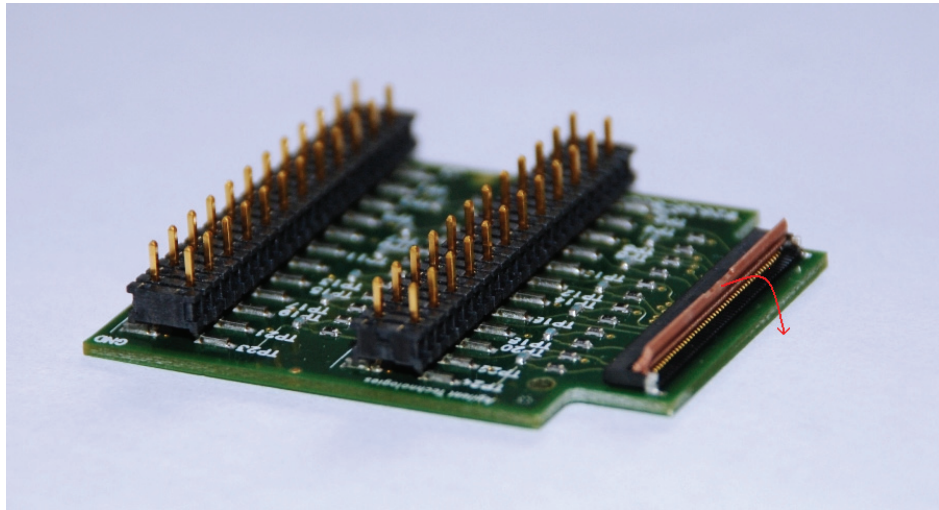


## Oscilloscope Connection to the W2637A/38A Series Probes

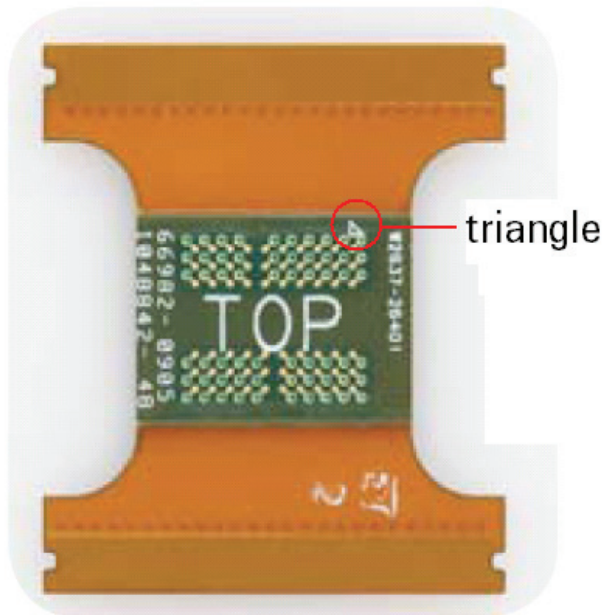
The LPDDR BGA probes are used with the Agilent E2678A socketed InfiniiMax probe head and the W2639A oscilloscope adapter boards to connect to an oscilloscope.

To connect to an oscilloscope, first solder the LPDDR BGA probe to the circuit board. Then attach the W2639A oscilloscope adapter boards to the “wings” of the LPDDR probes (two adapter boards for the W2637A (x16) probe and four for the W2638A (x32) probe). To attach these adapter boards to the wing, simply lift up on the ZIF connectors located on the probe, then insert the ZIF connector on the adapter board, and then close the probe ZIF connector to lock the assembly into position. The picture below shows the location of the ZIF connector as well as an arrow indicating how to close and lock the assembly into position.

## 2. Installing the LPDDR BGA Probes



Please note that the side labeled “TOP” on the LPDDR probes should be pointing upwards. Also, there is a small triangle in one of the corners (see picture below). This edge should be the top left corner.





Make sure you set the following values in the **Probe Setup** dialog box on your oscilloscope.

- Set the **Gain** setting by referring to the table / formula below. The voltage is halved due to termination resistors on the adapter board.

Transmitter Termination, Tx	Receiver Termination, Rx	Probe Gain Factor
100	100	0.24*, 0.20**
75	75	0.26*, 0.21**
50	50	0.27*, 0.22**

\*for W2637A/W2638A (see formulas below)

\*\*for W2631/32/33/34A and W3631/33A (see formulas below)

$$\text{Probe Gain Factor} = 60.4 / (x + y + 37.4 + 60.4)$$

where:

$$x = [(1/Tx) + (1/Rx)]^{-1}$$

y = 100 Ω for W2637A/W2638A

y = 150 Ω for W2631/32/33/34A and W3631/33A

- Make sure the DF Sckt probe head is selected in the **Head Label** field.

1 1169A 2 1169A 3 1169A 4 No Probe

Configure Probing System Calibrate Probe...

External Scaling

Units: Volt

Gain: 0.27:1

Ratio Decibel

Offset: 0.0 V

Head Label (Type): Head4 (E2678A:DF Sckt)

Add Head... Edit Head... Delete Head Delete ALL

Signal being probed: Differential

Head4 Model: E2678A Diff Socketed

1169A Probe Amplifier Serial #: US44002033 Bandwidth: 12.0 GHz

Probe System Calibration Status: Atten Cal: Uncalibrated Skew Cal: Uncalibrated Attenuation: 3.2:1

Characteristics: Bandwidth: 12.0 GHz Resistance: 50.0 kΩ Capacitance: 340.0 fF Max input: ±30.0 V Dyn range: ±1.7 V CM range: ±8.0 V SE offset range: ±16.0 V

Make sure the DF Sckt probe head is selected

Set the Gain Setting here. The voltage is reduced due to termination resistors on the adapter board.

## 2. Installing the LPDDR BGA Probes

### W2639A LPDDR BGA Probe Adapter Board Pin-Out for W2637A x16 LPDDR BGA Probe

Left Flex Wing						Right Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point	Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
GND	NC	TP1	GND	DQ14	TP2	TP24	DQ0	GND	TP23	DQ1	GND
GND	DQ15	TP3	GND	DQ13	TP4	TP22	DQ2	GND	TP21	DQ3	GND
GND	DQ12	TP5	GND	DQ10	TP6	TP20	GND	GND	TP19	DQ5	GND
GND	UDQS	TP7	GND	DQ9	TP8	TP18	CKE	GND	TP17	DQ6	GND
GND	DQ8	TP9	GND	DQ11	TP10	TP16	DQ4	GND	TP15	DQ7	GND
GND	UDM	TP11	GND	NC	TP12	TP14	CK	GND	TP13	RAS#	GND
GND	LDM	TP13	GND	LDQS	TP14	TP12	CK#	GND	TP11	WE#	GND
GND	BA0	TP15	GND	CS#	TP16	TP10	CAS#	GND	TP9	BA1	GND
GND	A9	TP17	GND	A6	TP18	TP8	A13	GND	TP7	A11	GND
GND	A7	TP19	GND	A8	TP20	TP6	A12, NC	GND	TP5	A1	GND
GND	A4	TP21	GND	A5	TP22	TP4	A0	GND	TP3	A10	GND
GND	NC	TP23	GND	NC	TP24	TP2	A3	GND	TP1	A2	GND

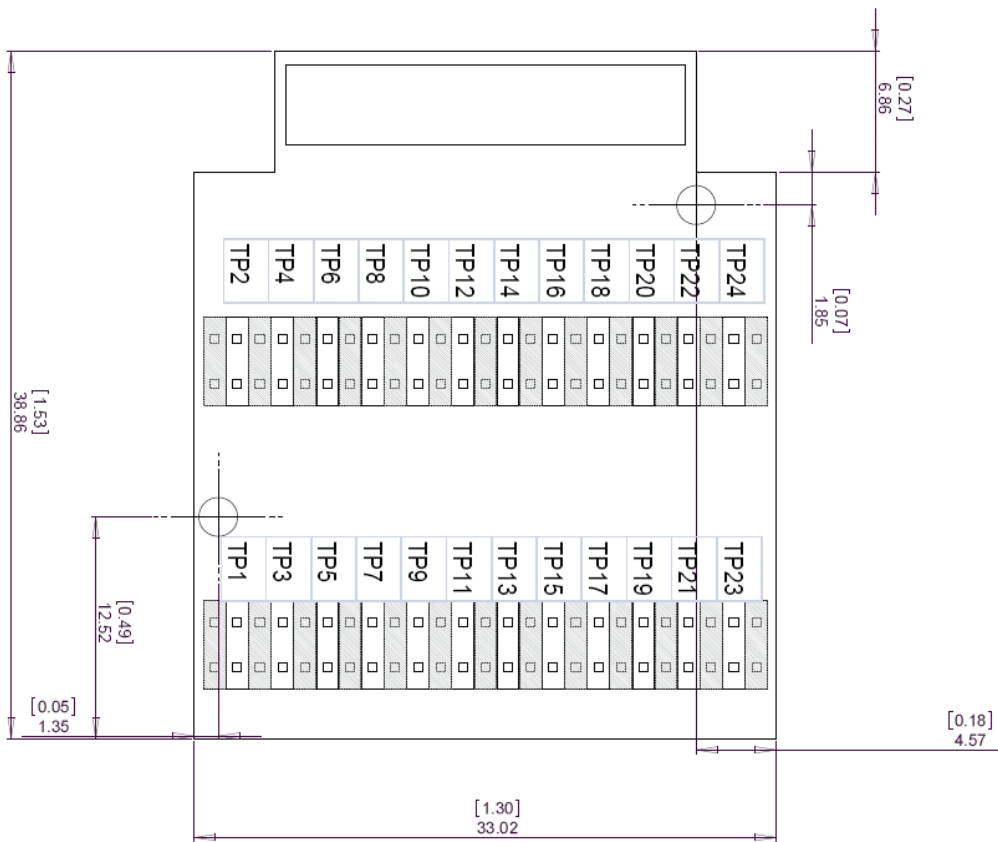
**W2639A LPDDR BGA Probe Adapter Board Pin-Out for W2638A x32 LPDDR BGA Probe**

Left Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point
GND	DM1	TP1	GND	DQ31	TP2
GND	DQ29	TP3	GND	DQ27	TP4
GND	DQ25	TP5	GND	DQ9	TP6
GND	DQS2	TP7	GND	DQ11	TP8
GND	DQ13	TP9	GND	DQ15	TP10
GND	DM2	TP11	GND	CAS#	TP12
GND	WE#	TP13	GND	RAS#	TP14
GND	DM1	TP15	GND	DQS1	TP16
GND	A9	TP17	GND	A12	TP18
GND	A11	TP19	GND	A6	TP20
GND	A7	TP21	GND	A8	TP22
GND	A4	TP23	GND	A5	TP24

Right Flex Wing					
Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
TP24	DQ16	GND	TP23	DQ18	GND
TP22	DQ20	GND	TP21	DQ22	GND
TP20	CKE	GND	TP19	DQ6	GND
TP18	GND	GND	TP17	DQ4	GND
TP16	DQ2	GND	TP15	DQ0	GND
TP14	CS#	GND	TP13	BA1	GND
TP12	GND	GND	TP11	BA0	GND
TP10	DM0	GND	TP9	DQS0	GND
TP8	NC	GND	TP7	NC	GND
TP6	NC	GND	TP5	A1	GND
TP4	A0	GND	TP3	A10/AP	GND
TP2	A3	GND	TP1	A2	GND

Bottom Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point
GND	NC	TP1	GND	DQ8	TP2
GND	DQ10	TP3	GND	DQ12	TP4
GND	DQ14	TP5	GND	DQ1	TP6
GND	NC	TP7	GND	DQ3	TP8
GND	DQ5	TP9	GND	DQ7	TP10
GND	NC	TP11	GND	NC	TP12
GND	NC	TP13	GND	NC	TP14
GND	NC	TP15	GND	NC	TP16
GND	NC	TP17	GND	NC	TP18
GND	NC	TP19	GND	NC	TP20
GND	NC	TP21	GND	NC	TP22
GND	NC	TP23	GND	NC	TP24

Top Flex Wing					
Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
TP24	DQ24	GND	TP23	DQ26	GND
TP22	DQ28	GND	TP21	DQ30	GND
TP20	CK#	GND	TP19	DQ17	GND
TP18	CK	GND	TP17	DQ19	GND
TP16	DQ21	GND	TP15	DQ23	GND
TP14	NC	GND	TP13	NC	GND
TP12	NC	GND	TP11	NC	GND
TP10	NC	GND	TP9	NC	GND
TP8	NC	GND	TP7	NC	GND
TP6	NC	GND	TP5	NC	GND
TP4	NC	GND	TP3	NC	GND
TP2	NC	GND	TP1	NC	GND



**W2639A LPDDR BGA Probe Adapter Board Pin-Out for DDR2 Interposer Configuration (W2633A) – see Appendix**

Left Flex Wing						Right Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point	Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
GND	NC	TP1	GND	NC	TP2	TP24	NC	GND	TP23	NC	GND
GND	NC	TP3	GND	NC	TP4	TP22	NC	GND	TP21	NC	GND
GND	NC	TP5	GND	DQ6	TP6	TP20	LDQS#	GND	TP19	DQ7	GND
GND	NC	TP7	GND	DQ1	TP8	TP18	LDQS	GND	TP17	DQ0	GND
GND	DQ3	TP9	GND	DQ4	TP10	TP16	DQ2	GND	TP15	DQ5	GND
GND	VREF	TP11	GND	CKE	TP12	TP14	CK	GND	TP13	ODT0	GND
GND	WE#	TP13	GND	BA1	TP14	TP12	CK#	GND	TP11	RAS#	GND
GND	BA0	TP15	GND	BA2	TP16	TP10	CAS#	GND	TP9	CS#	GND
GND	A1	TP17	GND	A5	TP18	TP8	A0	GND	TP7	A4	GND
GND	A10	TP19	GND	A3	TP20	TP6	A2	GND	TP5	A6	GND
GND	A7	TP21	GND	A9	TP22	TP4	A8	GND	TP3	RFU#2	GND
GND	A12	TP23	GND	NC	TP24	TP2	A11	GND	TP1	NC	GND

**W2639A LPDDR BGA Probe Adapter Board Pin-Out for DDR2 Interposer Configuration (W2631A)- see Appendix**

Left Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point
GND	UDM	TP1	GND	DQ14	TP2
GND	DQ9	TP3	GND	DQ11	TP4
GND	DQ12	TP5	GND	DQ6	TP6
GND	LDM	TP7	GND	DQ1	TP8
GND	DQ3	TP9	GND	DQ4	TP10
GND	VREF	TP11	GND	CKE	TP12
GND	WE#	TP13	GND	BA1	TP14
GND	BA0	TP15	GND	BA2	TP16
GND	A1	TP17	GND	A5	TP18
GND	A10	TP19	GND	A3	TP20
GND	A7	TP21	GND	NC	TP22
GND	A12	TP23	GND	A9	TP24

Right Flex Wing					
Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
TP24	DQ15	GND	TP23	DQ8	GND
TP22	DQ10	GND	TP21	DQ13	GND
TP20	LDQS#	GND	TP19	DQ7	GND
TP18	LDQS	GND	TP17	DQ0	GND
TP16	DQ2	GND	TP15	DQ5	GND
TP14	CK	GND	TP13	ODT	GND
TP12	CK#	GND	TP11	RAS#	GND
TP10	CAS#	GND	TP9	CS#	GND
TP8	A0	GND	TP7	A4	GND
TP6	A2	GND	TP5	A6	GND
TP4	A8	GND	TP3	RFU#2	GND
TP2	A11	GND	TP1	NC	GND

**W2639A LPDDR BGA Probe Adapter Board Pin-Out for DDR3 Interposer Configuration (W3633A)**

Left Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point
GND	DQ0	TP1	GND	DQ2	TP2
GND	DQS	TP3	GND	DQS#	TP4
GND	DQ6	TP5	GND	NC	TP6
GND	DQ4	TP7	GND	RAS#	TP8
GND	ODT1	TP9	GND	CAS#	TP10
GND	ODT0	TP11	GND	CS0#	TP12
GND	WE#	TP13	GND	CS1#	TP14
GND	BA2	TP15	GND	BA0	TP16
GND	A0	TP17	GND	A5	TP18
GND	A3	TP19	GND	A2	TP20
GND	A7	TP21	GND	GND	TP22
GND	RESET#	TP23	GND	A13	TP24

Right Flex Wing					
Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
TP24	NC	GND	TP23	NC	GND
TP22	NC	GND	TP21	NC	GND
TP20	NC	GND	TP19	DQ1	GND
TP18	DM	GND	TP17	DQ3	GND
TP16	DQ7	GND	TP15	DQ5	GND
TP14	CK	GND	TP13	CKE1	GND
TP12	CK#	GND	TP11	CKE0	GND
TP10	A10/AP	GND	TP9	A15	GND
TP8	A12/BC#	GND	TP7	A4	GND
TP6	BA1	GND	TP5	A1	GND
TP4	A6	GND	TP3	A11	GND
TP2	A8	GND	TP1	A14	GND

**W2639A LPDDR BGA Probe Adapter Board Pin-Out for DDR3 Interposer Configuration (W3631A)**

## 2. Installing the LPDDR BGA Probes

Left Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point
GND	DQU7	TP1	GND	DQU5	TP2
GND	DQU1	TP3	GND	DQU3	TP4
GND	DQL0	TP5	GND	DQL6	TP6
GND	DQL2	TP7	GND	DQL4	TP8
GND	ODT1	TP9	GND	RAS#	TP10
GND	ODT0	TP11	GND	CS0#	TP12
GND	CAS#	TP13	GND	CS1#	TP14
GND	WE#	TP15	GND	BA0	TP16
GND	A3	TP17	GND	A5	TP18
GND	A0	TP19	GND	A2	TP20
GND	A7	TP21	GND	A9	TP22
GND	RESET	TP23	GND	A13	TP24

Right Flex Wing					
Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
TP24	DQU4	GND	TP23	DQU6	GND
TP22	DQSU#	GND	TP21	DQSU	GND
TP20	DQU2	GND	TP19	DML	GND
TP18	DQU0	GND	TP17	DQL1	GND
TP16	DQL3	GND	TP15	DQL7	GND
TP14	DQL5	GND	TP13	CK#	GND
TP12	CK	GND	TP11	CKE1	GND
TP10	CKE0	GND	TP9	A10/AP	GND
TP8	A12/BC#	GND	TP7	A4	GND
TP6	BA1	GND	TP5	A1	GND
TP4	A6	GND	TP3	A11	GND
TP2	A8	GND	TP1	A14	GND

### 3. Setting Up the Logic Analysis System

The mapping of specific signals to logic analyzer channels depends on:

- Which DRAMs on a DIMM are probed
- Which probe you are using
- How the single ended logic analyzer cable adapters are arranged when connecting to the LPDDR DRAM BGA probes

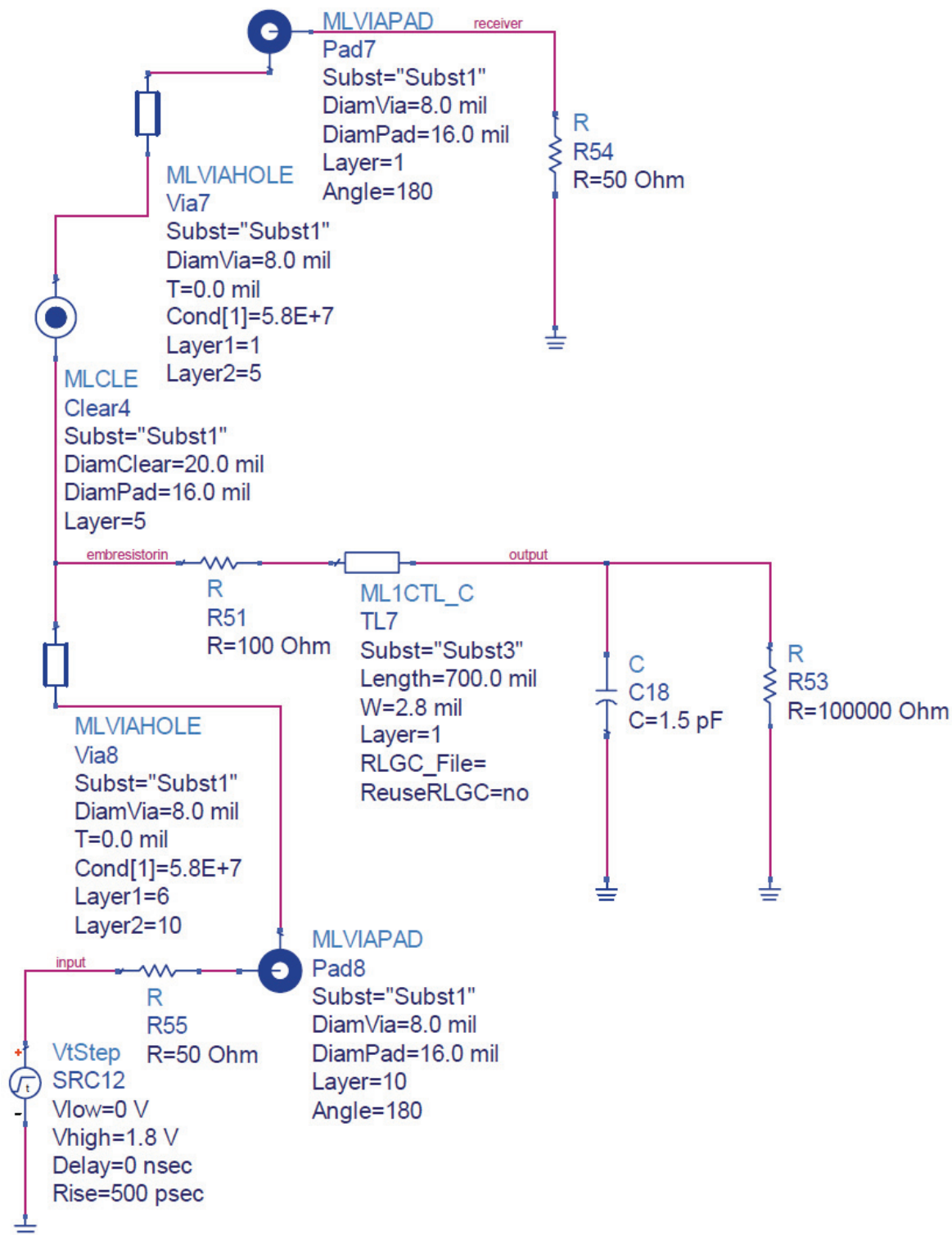
Because of these dependencies, there is no single logic analyzer configuration file setup, and no configuration file is supplied with the probes. The logic analyzer Buses/Signals setup dialog will allow you to assign descriptive labels to each analyzer channel that associate each channel with the particular DRAM and DRAM signal being probed.

#### **To Save a Configuration File**

After you set up the logic analyzer, it is strongly recommended that you save the configuration.

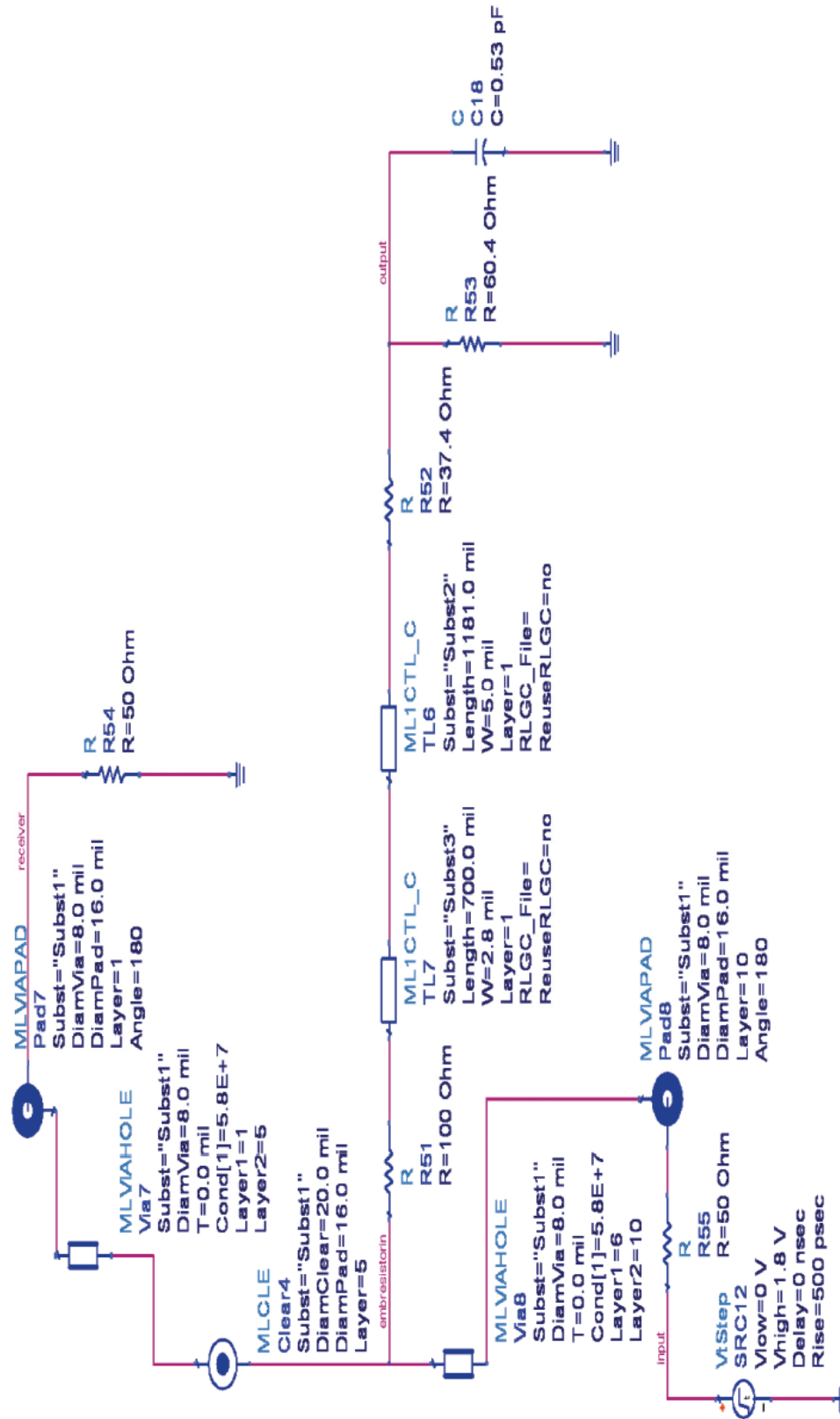
To save your work, select **File > Save As ...** and save the configuration as an ALA format file. ALA format configuration files are more complete and efficient than XML format configuration files. See the logic analyzer online help for more information on these formats.

### 4. Characteristics, Regulatory, and Safety Information



W2637A and W2638A Probes with logic analyzer cable (E5384A/E5826A)





W2637A and W2638A Probes with W2639A Oscilloscope Adapter Board

#### 4. Characteristics, Regulatory, and Safety Information

### Spice Decks for W2637A and W2638A Probes

```
*****
***
***      LPDDR Interposer + Logic Analyzer Cable (E5384A/E5826A/E5827A) SPICE Model
***
*****
```

\*bb spice subcircuit with consecutive port numbers.

.SUBCKT bb spice\_LAcablelpddr\_subckt port\_1 port\_2 gnd\_0

\* PORT\_1

```
vi_1 port_1 _net_1 0.000000000000e+000
vb_1 _net_4 _net_5 0.000000000000e+000
R_Z0_1 _net_1 _net_2 5.000000000000e+001 NOISE=0
H_b_1 _net_2 gnd_0 vb_1 1.41421356237310e+001
E_v_1 _net_3 gnd_0 port_1 gnd_0 7.07106781186548e-002
H_i_1 _net_4 _net_3 vi_1 3.53553390593274e+000
```

```
G_C_1_1 _net_5 gnd_0 _net_11 gnd_0 -3.22608552467231e+009
G_C_1_2 _net_5 gnd_0 _net_12 gnd_0 -1.85622867007219e+009
G_C_1_3 _net_5 gnd_0 _net_13 gnd_0 -4.24046553324636e+009
G_C_1_4 _net_5 gnd_0 _net_14 gnd_0 -4.25728470875830e+009
G_C_1_5 _net_5 gnd_0 _net_15 gnd_0 1.05067661912510e+010
G_C_1_6 _net_5 gnd_0 _net_16 gnd_0 -6.49079078505455e+009
G_C_1_7 _net_5 gnd_0 _net_17 gnd_0 3.08198380221454e+009
G_C_1_8 _net_5 gnd_0 _net_18 gnd_0 7.23969632915889e+009
```

\* PORT\_2

```
vi_2 port_2 _net_6 0.000000000000e+000
vb_2 _net_9 _net_10 0.000000000000e+000
R_Z0_2 _net_6 _net_7 5.000000000000e+001 NOISE=0
H_b_2 _net_7 gnd_0 vb_2 1.41421356237310e+001
E_v_2 _net_8 gnd_0 port_2 gnd_0 7.07106781186548e-002
H_i_2 _net_9 _net_8 vi_2 3.53553390593274e+000
```

```
G_C_2_1 _net_10 gnd_0 _net_11 gnd_0 1.05067661912510e+010
G_C_2_2 _net_10 gnd_0 _net_12 gnd_0 -6.49079078505455e+009
G_C_2_3 _net_10 gnd_0 _net_13 gnd_0 3.08198380221454e+009
G_C_2_4 _net_10 gnd_0 _net_14 gnd_0 7.23969632915889e+009
G_C_2_5 _net_10 gnd_0 _net_15 gnd_0 3.82698652097210e+010
G_C_2_6 _net_10 gnd_0 _net_16 gnd_0 -5.59332217972397e+010
G_C_2_7 _net_10 gnd_0 _net_17 gnd_0 -1.12021520702025e+010
G_C_2_8 _net_10 gnd_0 _net_18 gnd_0 -6.74361603121270e+009
```

\* STATE\_1

```
C_1 _net_11 gnd_0 1.000000000000e-011
G_A_1_1 _net_11 gnd_0 _net_11 gnd_0 1.34401797487851e-001
G_B_1_1 _net_11 gnd_0 _net_4 gnd_0 -1.000000000000e-011
```

\* STATE\_2

```
C_2 _net_12 gnd_0 1.000000000000e-011
G_A_2_2 _net_12 gnd_0 _net_12 gnd_0 2.47566797545524e-001
G_B_2_1 _net_12 gnd_0 _net_4 gnd_0 -1.000000000000e-011
```

\* STATE\_3

```
C_3 _net_13 gnd_0 1.000000000000e-011
G_A_3_3 _net_13 gnd_0 _net_13 gnd_0 1.64751890165784e-001
G_A_3_4 _net_13 gnd_0 _net_14 gnd_0 -6.43501358659259e-001
G_B_3_1 _net_13 gnd_0 _net_4 gnd_0 -2.000000000000e-011
```

\* STATE\_4

```
C_4 _net_14 gnd_0 1.000000000000e-011
G_A_4_4 _net_14 gnd_0 _net_14 gnd_0 1.64751890165784e-001
G_A_4_3 _net_14 gnd_0 _net_13 gnd_0 6.43501358659259e-001
```

```
* STATE_5
C_5 _net_15 gnd_0 1.000000000000000e-011
G_A_5_5 _net_15 gnd_0 _net_15 gnd_0 1.34401797487851e-001
G_B_5_2 _net_15 gnd_0 _net_9 gnd_0 -1.000000000000000e-011
```

```
* STATE_6
C_6 _net_16 gnd_0 1.000000000000000e-011
G_A_6_6 _net_16 gnd_0 _net_16 gnd_0 2.47566797545524e-001
G_B_6_2 _net_16 gnd_0 _net_9 gnd_0 -1.000000000000000e-011
```

```
* STATE_7
C_7 _net_17 gnd_0 1.000000000000000e-011
G_A_7_7 _net_17 gnd_0 _net_17 gnd_0 1.64751890165784e-001
G_A_7_8 _net_17 gnd_0 _net_18 gnd_0 -6.43501358659259e-001
G_B_7_2 _net_17 gnd_0 _net_9 gnd_0 -2.000000000000000e-011
```

```
* STATE_8
C_8 _net_18 gnd_0 1.000000000000000e-011
G_A_8_8 _net_18 gnd_0 _net_18 gnd_0 1.64751890165784e-001
G_A_8_7 _net_18 gnd_0 _net_17 gnd_0 6.43501358659259e-001
```

```
.ENDS bbspice_LAcablelppdr_subckt
*****
```

```
*****
* S-based subckt
```

```
*bbsplice subcircuit with external port numbers.
```

```
.SUBCKT bbspice_LAcablelppdr 1 2 0
x_ 1 2 0 bbspice_LAcablelppdr_subckt
```

```
.ENDS bbspice_LAcablelppdr
*****
```

#### 4. Characteristics, Regulatory, and Safety Information

```
*****  
***  
***  
***  
*****  
***  
*****
```

#### LPDDR Interposer + W2639A SPICE Model

\*bb spice subcircuit with consecutive port numbers.

```
.SUBCKT bb spice_syslpddr_subckt port_1 port_2 gnd_0
```

\* PORT\_1

```
vi_1 port_1 _net_1 0.0000000000000e+000  
vb_1 _net_4 _net_5 0.0000000000000e+000  
R_Z0_1 _net_1 _net_2 5.0000000000000e+001 NOISE=0  
H_b_1 _net_2 gnd_0 vb_1 1.41421356237310e+001  
E_v_1 _net_3 gnd_0 port_1 gnd_0 7.07106781186548e-002  
H_i_1 _net_4 _net_3 vi_1 3.53553390593274e+000
```

```
G_C_1_1 _net_5 gnd_0 _net_11 gnd_0 1.24005027897216e+009  
G_C_1_2 _net_5 gnd_0 _net_12 gnd_0 -1.56329103409242e+009  
G_C_1_3 _net_5 gnd_0 _net_13 gnd_0 -2.43281969714982e+009  
G_C_1_4 _net_5 gnd_0 _net_14 gnd_0 2.45669672903938e+010  
G_C_1_5 _net_5 gnd_0 _net_15 gnd_0 -2.52103573644686e+009  
G_C_1_6 _net_5 gnd_0 _net_16 gnd_0 -6.13849694652838e+009  
G_C_1_7 _net_5 gnd_0 _net_17 gnd_0 4.55445764882538e+009  
G_C_1_8 _net_5 gnd_0 _net_18 gnd_0 6.49291629738857e+010
```

\* PORT\_2

```
vi_2 port_2 _net_6 0.0000000000000e+000  
vb_2 _net_9 _net_10 0.0000000000000e+000  
R_Z0_2 _net_6 _net_7 5.0000000000000e+001 NOISE=0  
H_b_2 _net_7 gnd_0 vb_2 1.41421356237310e+001  
E_v_2 _net_8 gnd_0 port_2 gnd_0 7.07106781186548e-002  
H_i_2 _net_9 _net_8 vi_2 3.53553390593274e+000
```

```
G_C_2_1 _net_10 gnd_0 _net_11 gnd_0 -2.52103573644686e+009  
G_C_2_2 _net_10 gnd_0 _net_12 gnd_0 -6.13849694652838e+009  
G_C_2_3 _net_10 gnd_0 _net_13 gnd_0 4.55445764882538e+009  
G_C_2_4 _net_10 gnd_0 _net_14 gnd_0 6.49291629738857e+010  
G_C_2_5 _net_10 gnd_0 _net_15 gnd_0 -1.11104456711947e+010  
G_C_2_6 _net_10 gnd_0 _net_16 gnd_0 1.89160369519661e+010  
G_C_2_7 _net_10 gnd_0 _net_17 gnd_0 -3.48001162309017e+009  
G_C_2_8 _net_10 gnd_0 _net_18 gnd_0 -4.14924945810738e+011
```

\* STATE\_1

```
C_1 _net_11 gnd_0 1.0000000000000e-011  
G_A_1_1 _net_11 gnd_0 _net_11 gnd_0 9.58822912609048e-002  
G_A_1_2 _net_11 gnd_0 _net_12 gnd_0 -7.04839193299830e-002  
G_B_1_1 _net_11 gnd_0 _net_4 gnd_0 -2.0000000000000e-011
```

\* STATE\_2

```
C_2 _net_12 gnd_0 1.0000000000000e-011  
G_A_2_2 _net_12 gnd_0 _net_12 gnd_0 9.58822912609048e-002  
G_A_2_1 _net_12 gnd_0 _net_11 gnd_0 7.04839193299830e-002
```

\* STATE\_3

```
C_3 _net_13 gnd_0 1.0000000000000e-011  
G_A_3_3 _net_13 gnd_0 _net_13 gnd_0 2.01712271022166e-001  
G_A_3_4 _net_13 gnd_0 _net_14 gnd_0 -1.81352782179138e-002  
G_B_3_1 _net_13 gnd_0 _net_4 gnd_0 -2.0000000000000e-011
```

\* STATE\_4

```
C_4 _net_14 gnd_0 1.0000000000000e-011  
G_A_4_4 _net_14 gnd_0 _net_14 gnd_0 2.01712271022166e-001
```

```

G_A_4_3 _net_14 gnd_0 _net_13 gnd_0 1.81352782179138e-002
* STATE_5
C_5 _net_15 gnd_0 1.00000000000000e-011
G_A_5_5 _net_15 gnd_0 _net_15 gnd_0 9.58822912609048e-002
G_A_5_6 _net_15 gnd_0 _net_16 gnd_0 -7.04839193299830e-002
G_B_5_2 _net_15 gnd_0 _net_9 gnd_0 -2.00000000000000e-011
* STATE_6
C_6 _net_16 gnd_0 1.00000000000000e-011
G_A_6_6 _net_16 gnd_0 _net_16 gnd_0 9.58822912609048e-002
G_A_6_5 _net_16 gnd_0 _net_15 gnd_0 7.04839193299830e-002
* STATE_7
C_7 _net_17 gnd_0 1.00000000000000e-011
G_A_7_7 _net_17 gnd_0 _net_17 gnd_0 2.01712271022166e-001
G_A_7_8 _net_17 gnd_0 _net_18 gnd_0 -1.81352782179138e-002
G_B_7_2 _net_17 gnd_0 _net_9 gnd_0 -2.00000000000000e-011
* STATE_8
C_8 _net_18 gnd_0 1.00000000000000e-011
G_A_8_8 _net_18 gnd_0 _net_18 gnd_0 2.01712271022166e-001
G_A_8_7 _net_18 gnd_0 _net_17 gnd_0 1.81352782179138e-002

```

```

.ENDS bbspice_syslpddr_subckt
*****

```

```

*****
* S-based subckt

```

```

*bbspice subcircuit with external port numbers.

```

```

.SUBCKT bbspice_syslpddr          1      2      0
x_      1      2      0      bbspice_syslpddr_subckt

```

```

.ENDS bbspice_syslpddr
*****

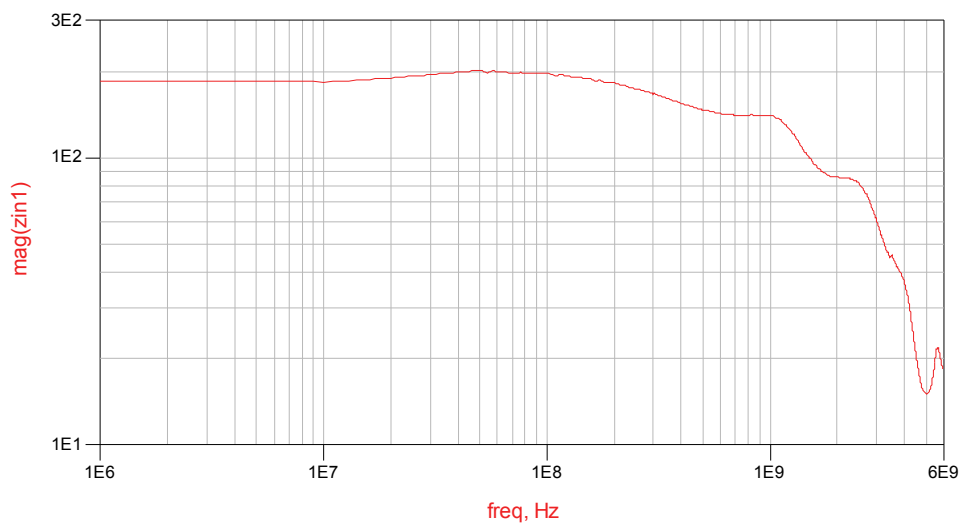
```

## Electrical Characteristics

The following electrical characteristics are not specifications, but are typical electrical characteristics.

**Table 1** Electrical characteristics

<b>Operating Transfer Rate</b>	W2637A + E5384/E5826: 255 Mb/s W2638A + E5384/E5826: 255 Mb/s W2637A + W2639A: 500 Mb/s W2638A + W2639A: 500 Mb/s
<b>Bandwidth (3 dB)</b>	W2637A + E5384/E5826: 510 MHz W2638A + E5384/E5826: 510 MHz W2637A + W2639A: 1.5 GHz W2638A + W2639A: 1.5 GHz
<b>Rise time</b>	W2637A + E5384/E5826: 686 ps W2638A + E5384/E5826: 686 ps W2637A + W2639A: 233 ps W2638A + W2639A: 233 ps
<b>Input Impedance</b>	W2637A + W2639A: 200 $\Omega$ W2638A + W2639A: 200 $\Omega$



**Input impedance of W2637A/W2638A with W2639A Oscilloscope Adapter Board**

## Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis of the W2637A and W2638A probes with the oscilloscope probe.

**Table 2** Environmental characteristics (Operating)

<b>Temperature</b>	0° to + 100° C
<b>Altitude</b>	4,600 m (15,000 ft)
<b>Humidity</b>	Up to 50% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only.

## Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

## Warnings

Use only the recommended power supply.

If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

If it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do not install substitute parts or perform any unauthorized modification to the instrument.

Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

#### 4. Characteristics, Regulatory, and Safety Information

Do not use the instrument in a manner not specified by the manufacturer.

#### Safety Symbols



Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.



Hazardous voltage symbol



Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis

#### Regulatory Information



China RoHS non-restricted for W2637A, W2638A, and W2639A



China RoHS restricted for E5384, E5826/7





## Appendix A: W2639A Rework Instruction Guide – For use when W2639A Oscilloscope Probe Adapter Board is used with DDR2 BGA probe (W2631A and W2633A)

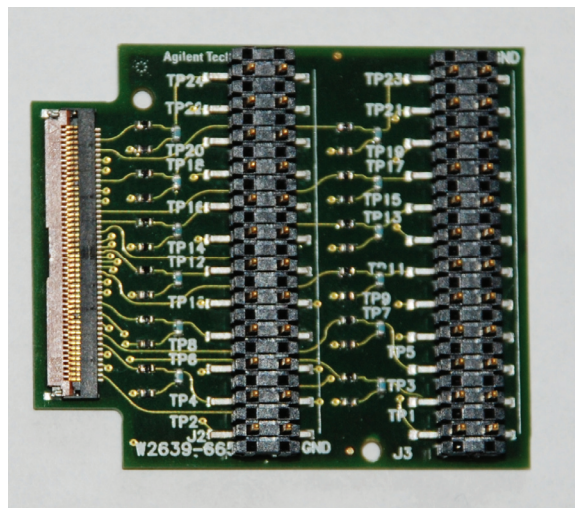
### Introduction

This appendix provides rework information for the following Agilent product:

- W2639A Oscilloscope Probe Adapter Board

The W2639A is designed to provide high bandwidth performance to the oscilloscope with proper termination. However, for use with the DDR2 BGA probe, the VREF point should not be terminated. The rework instructions provide a workaround to correct the termination point of VREF on the W2639A Oscilloscope Probe Adapter Board.

The figure below shows the W2639A Oscilloscope Probe Adapter Board.



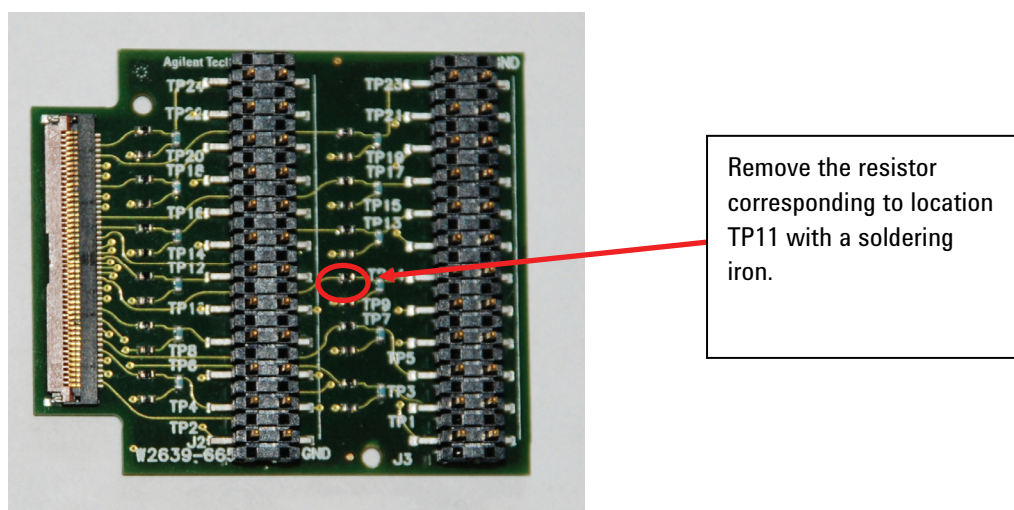
W2639A Oscilloscope Probe Adapter Board

### Equipment Required for Rework

- W2639A Oscilloscope Probe Board Adapter (1 of 2)
- Soldering iron

## Rework Instructions to Remove VREF Termination on W2639A DDR2 Oscilloscope Adapter Board When Used With W2631A DDR2 x16 BGA Probe

1. The VREF signal is connected to the W2639A Oscilloscope Probe Adapter Board via the left flex wing of the W2631A DDR2 BGA probe on TP11 as shown in the table on the next page.
2. Remove the 37.4 ohm resistor located near TP11 with a soldering iron as shown in the figure below to disconnect the signal from GND. This will open the path to VREF.



Location of the 37.4ohm resistor for TP11 on the W2639A Oscilloscope Probe Adapter Board

3. Label the reworked W2639A Oscilloscope Probe Adapter Board “LEFT”. The reworked W2639A must only connect to the left flex wing of the W2631A DDR2 BGA probe.
4. The rework instructions may be repeated for the following BGA probes with reference to the pin-out tables shown in earlier sections of this user’s guide.
  - W2631A x16 DDR2 BGA probe
  - W2633A x8 DDR2 BGA probe

*Note: Please contact Agilent to confirm the exact location of the resistor.*

W2639A BGA scope probe adapter pin-out for W2631A

Left Flex Wing						
Signal Name	Signal Name	Test Point		Signal Name	Signal Name	Test Point
GND	UDM	TP1		GND	DQ14	TP2
GND	DQ9	TP3		GND	DQ11	TP4
GND	DQ12	TP5		GND	DQ6	TP6
GND	LDM	TP7		GND	DQ1	TP8
GND	DQ3	TP9		GND	DQ4	TP10
<b>GND</b>	<b>VREF</b>	<b>TP11</b>		GND	CKE	TP12
GND	WE#	TP13		GND	BA1	TP14
GND	BA0	TP15		GND	BA2	TP16
GND	A1	TP17		GND	A5	TP18
GND	A10	TP19		GND	A3	TP20
GND	A7	TP21		GND	NC	TP22
GND	A12	TP23		GND	A9	TP24

Right Flex Wing						
Test Point	Signal Name	Signal Name		Test Point	Signal Name	Signal Name
TP24	DQ15	GND		TP23	DQ8	GND
TP22	DQ10	GND		TP21	DQ13	GND
TP20	LDQS#	GND		TP19	DQ7	GND
TP18	LDQS	GND		TP17	DQ0	GND
TP16	DQ2	GND		TP15	DQ5	GND
TP14	CK	GND		TP13	ODT	GND
TP12	CK#	GND		TP11	RAS#	GND
TP10	CAS#	GND		TP9	CS#	GND
TP8	A0	GND		TP7	A4	GND
TP6	A2	GND		TP5	A6	GND
TP4	A8	GND		TP3	RFU#2	GND
TP2	A11	GND		TP1	NC	GND

*Manual Part Number W2638-97001*

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